



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/817,548
Filing Date April 2, 2004
Inventor Martin Ceredig Roberts et al.
Assignee Micron Technology, Inc.
Group Art Unit 2814
Examiner Peralta, Ginette
Attorney's Docket No. MI22-2550
Title: Methods of Forming Capacitors, and Methods of Forming DRAM
Circuitry

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References –See Attached Form PTO-1449

The attached Form PTO/SB/08a is submitted in compliance with 37 CFR §1.56. Pursuant to FEDERAL REGISTER, Vol. 69, No. 182, pg. 56542 (September 21, 2004), no copies of any cited U.S. patents or U.S. published applications are included herewith. Copies of all other cited art are attached. No admission is made regarding whether the listed references are prior art.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: December 15, 2005

By: Jennifer J. Taylor
Jennifer J. Taylor, Ph.D.
Reg. No. 48,711

EV 633202625

CLIPPEDIMAGE= DE004213945A1

PUB-NO: DE004213945A1

DOCUMENT-IDENTIFIER: DE 4213945 A1

TITLE: Memory capacitor in semiconductor device for DRAM cells -
comprises

conductively doped poly:silicon@ layers and insulating layer comprising
capacitor dielectric adjacent to memory node of 2nd poly:sil

PUBN-DATE: November 5, 1992

INVENTOR-INFORMATION:

NAME	COUNTRY
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FAZAN, PIERRE	US
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CHAN, HIANG C	US
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ASSIGNEE-INFORMATION:

NAME	COUNTRY
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MICRON TECHNOLOGY INC	US
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APPL-NO: DE04213945

APPL-DATE: April 28, 1992

PRIORITY-DATA: US69285991A (April 29, 1991)

INT-CL_(IPC): H01L021/72; H01L027/108

EUR-CL (EPC): H01L027/108

US-CL-CURRENT: 257/307

ABSTRACT:

A memory capacitor has (1) a conductively doped first polysilicon layer with
a
first and a second end, the first end making contact with a memory node
connection of an access device and the second end being insulated from an
adjacent conductive material by a dielectric; (2) a conductively doped second
polysilicon layer adhering to the first polysilicon layer, forming a memory
node plate of I-shaped cross-section; (3) an insulating layer comprising a
capacitor dielectric adjacent to the memory node plate and extending the
same

distance as the latter except for regions for the contact point at its first end and the insulation at its second end; and (4) a conductively doped third polysilicon layer forming a cell plate which has an upper and a lower surface, and adjacent to and of the same extent as the capacitor dielectric layer.

The

doped polysilicon is pref. produced by gas-phase deposition, as are all the dielectric layers. The capacitor dielectric layer is selected from nitrides, oxidised nitrides, Ta₂O₅, oxidised Ta₂O₅ and SrTiO₃. USE/ADVANTAGE -

Used in

the mfr. of DRAM, VRAM and other stacked memory cell devices. Capacitor maximises the memory cell active surface in the prodn. of high-density DRAMs

(an increase of 200% or more is quoted).